CHI MEI OPTOELECTRONICS CORP.

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Model No.: V562D1-L01
Preliminary

TFT LCD Preliminary Specification

MODEL NO.: V562D1 - L01

LCD TV Division	
AVP	郭振隆

Liquid Crystal Display Division			
QRA Dept.	TVHD/PDD		
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Version1.0

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 1.0	Mar.02,'06	All	All	Preliminary Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V562D1-L01 is a 56" thin-film-transistor liquid-crystal (TFT-LCD) module with 32-CCFL Backlight unit and 2 ports – Dual DVI interface. This module supports 3840 x 2160 Quad Full High Definition (QFHD) TV format and can display true 16.7M colors (8-bit/colors). The inverter module for backlight is built-in.

1.2 FEATURES

- Ultra wide viewing angle (176(H)/ 176(V) for CR>30)
- High brightness (500 nits)
- High contrast ratio (1200:1)
- Ultra fast response time (Gray to gray average 6.5 ms)
- High color saturation (NTSC 75%)
- QFHD (3840 x 2160 pixels) resolution
- 2 ports – Dual DVI (Digital Visual Interface)
- RoHS compliance

1.3 APPLICATION

- Luxurious living room TVs.
- Public display.
- Home theater application.
- Satellite communication application.
- Medical treatment application.
- Security and monitoring application.
- Industrial design application.
- Multi-media display.

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	1244.16 (H) x 699.84 (V) (56.2" diagonal)	mm	
Bezel Opening Area	1252.1 (H) x 707.8 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	3840x R.G.B. x 2160	pixel	-
Pixel Pitch(Sub Pixel)	0.108 (H) x 0.324 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Hard coating 3H Low reflection coating< 2% reflection	-	(1)

Note (1) The spec of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	1308.5	1309.5	1310.8	mm	
	Vertical(V)	766	767	768.3	mm	
	Depth(D)	57.2	58.5	59.8	mm	To PCB cover
	Depth(D)	61.9	63.2	64.5	mm	To inverter cover
Weight		23000	23500	24000	g	

2. ABSOLUTE MAXIMUM RATING

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol		Value		Unit	Note
			Min.	Max.		
Storage Temperature	T_{ST}		-20	+55	ºC	(1)
Operating Ambient Temperature	T_{OP}		0	40	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	X, Y axis	-	30	G	(3), (5)
		Z axis	-	30	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}		-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

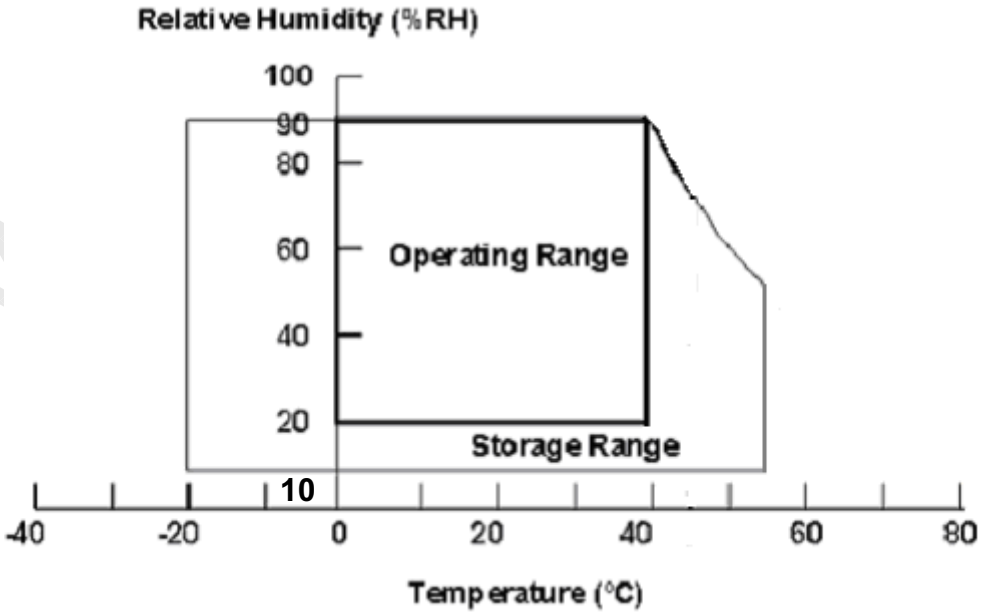
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in your product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, and ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture. The module would not be twisted or bent by the fixture.



3. ELECTRICAL MAXIMUM RATINGS

3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC1}	-0.3	20	V	
	V_{CC2}	-0.3	6	V	
DVI Termination Supply Voltage	AVcc		4.0	V	(2)
DVI Signal Voltage on any pin	-	-0.5	4.0	V	
DVI Differential Mode Signal Voltage on any pin	-	-0.5	4.0	V	

Note: (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under normal operating conditions.

(2) The maximum ratings of the DVI interface are specified in the DVI interface specification of DDWG.

3.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	5000	V_{RMS}	
Power Supply Voltage	V_{BL}	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(2), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals includes On/Off Control, Internal PWM Control, External PWM Control and Internal/External PWM Selection.

4. ELECTRICAL CHARACTERISTICS

4.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC1}	16.2	18	19.8	V	(1)
		V_{CC2}	4.5	5	5.5	V	
Power Supply Ripple Voltage		V_{RP1},V_{RP2}	-	-	200	mV	
Rush Current		I_{RUSH1}	-	-	4.5	A	
		I_{RUSH2}	-	-	5.0	A	
Power Supply Current	White	I_{CC1}	-	2	2.6	A	(3)
	Black		-	1	-	A	
	Vertical Stripe		-	1.8	-	A	
	White	I_{CC2}	-	2.6	-	A	
	Black		-	2.6	-	A	
	Vertical Stripe		-	3	3.5	A	
DVI Interface	Differential Input High Voltage	V_{LVTH}	+150	-	+1200	mV	(2)
	Differential Input Low Voltage	V_{LVTL}	-150	-	-1200	mV	
	Common Input Voltage	V_{LVC}	0.15	-	1.56	V	
	Reciver Resistor	R_T	95	100	105	ohm	

Note: (1)The module should be always operated within the above ranges.

(2)The electrical characteristics of the DVI interface are specified in the DVI interface specification of DDWG.

(3)The specified power supply current is under the conditions at Vcc1 = 18 V, Vcc2 = 5 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

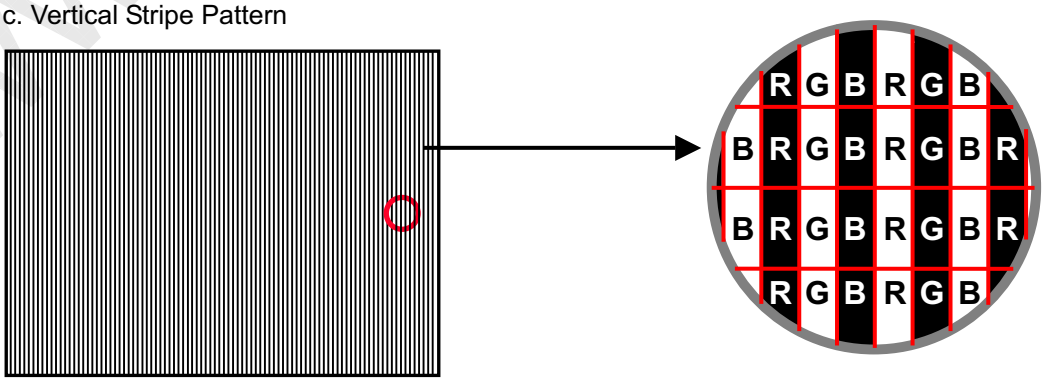
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

4.2 BACKLIGHT UNIT

4.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta=25±2℃)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Voltage	V_W	-	1720	-	V_{RMS}	I_L =6.5mA
Lamp Current	I_L	-	6.5	-	mA_{RMS}	(1)
Lamp Starting Voltage	V_S	-	-	2550	V_{RMS}	(2), Ta = 0 ºC
		-	-	2350	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_o	40	60	80	KHz	(3)
Lamp Life Time	L_{BL}	-	50000	-	Hrs	(4)

4.2.2 INVERTER CHARACTERISTICS (Ta=25±2℃)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	360	378	W	(5), I_L = 6.5mA
Power Supply Voltage	V_{BL}	22.8	24.0	25.2	V_{DC}	
Power Supply Current	I_{BL}	-	15	-	A	Non Dimming
Input Ripple Noise	-	-	-	500	mV_{P-P}	V_{BL}=22.8V
Backlight Turn on Voltage	V_{BS}	2550	-	-	V_{RMS}	Ta = 0 ºC
		2350	-	-	V_{RMS}	Ta = 25 ºC
Oscillating Frequency	F_W	47	50	53	kHz	
Dimming frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	-	20	-	%	

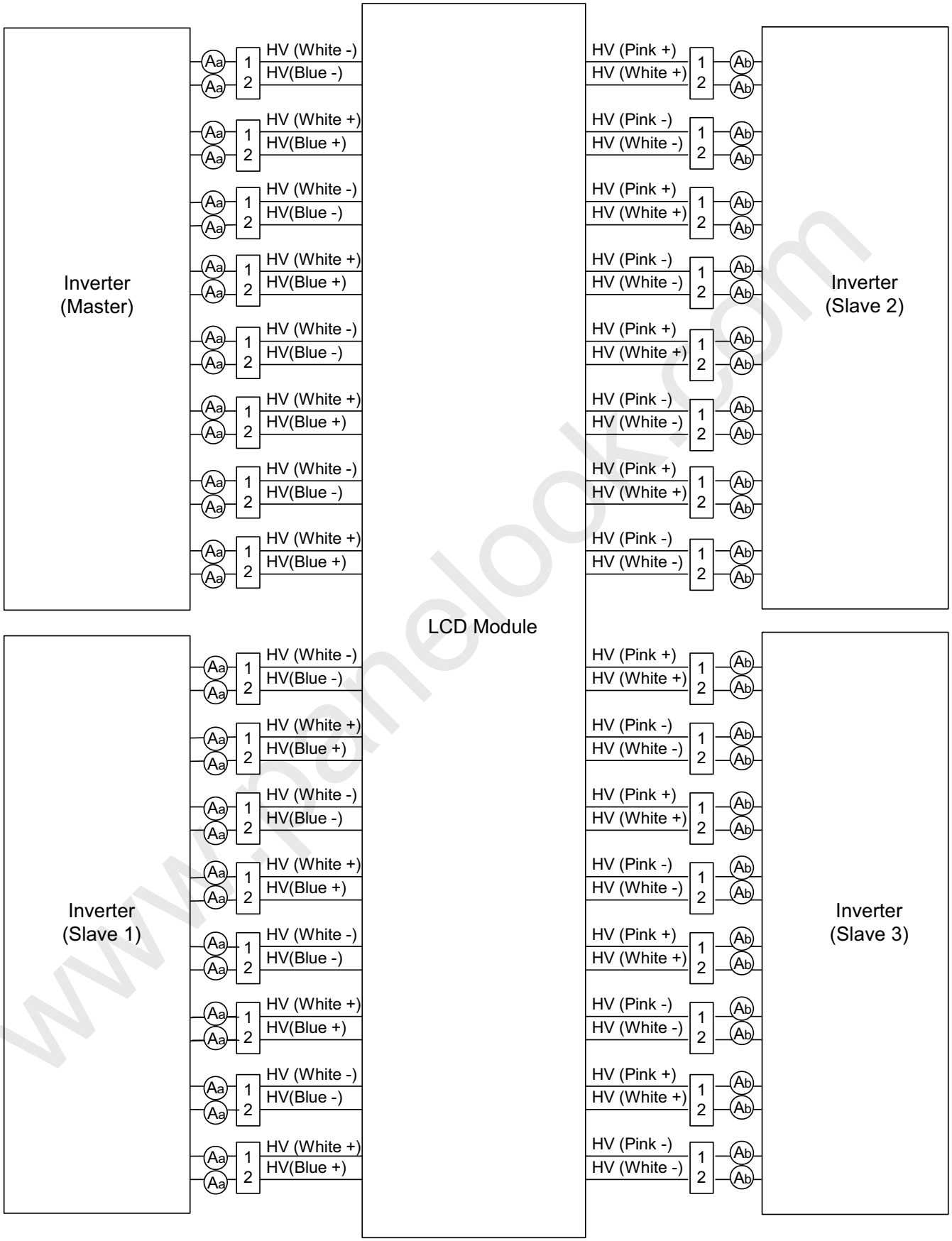
Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:

Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and I_L = 6.0 ~ 7.0 mArms.

Note (5) The measurement condition of Max. value is based on 56" backlight unit under input voltage 24V, average lamp current 6.8 mA and lighting 30 minutes later.



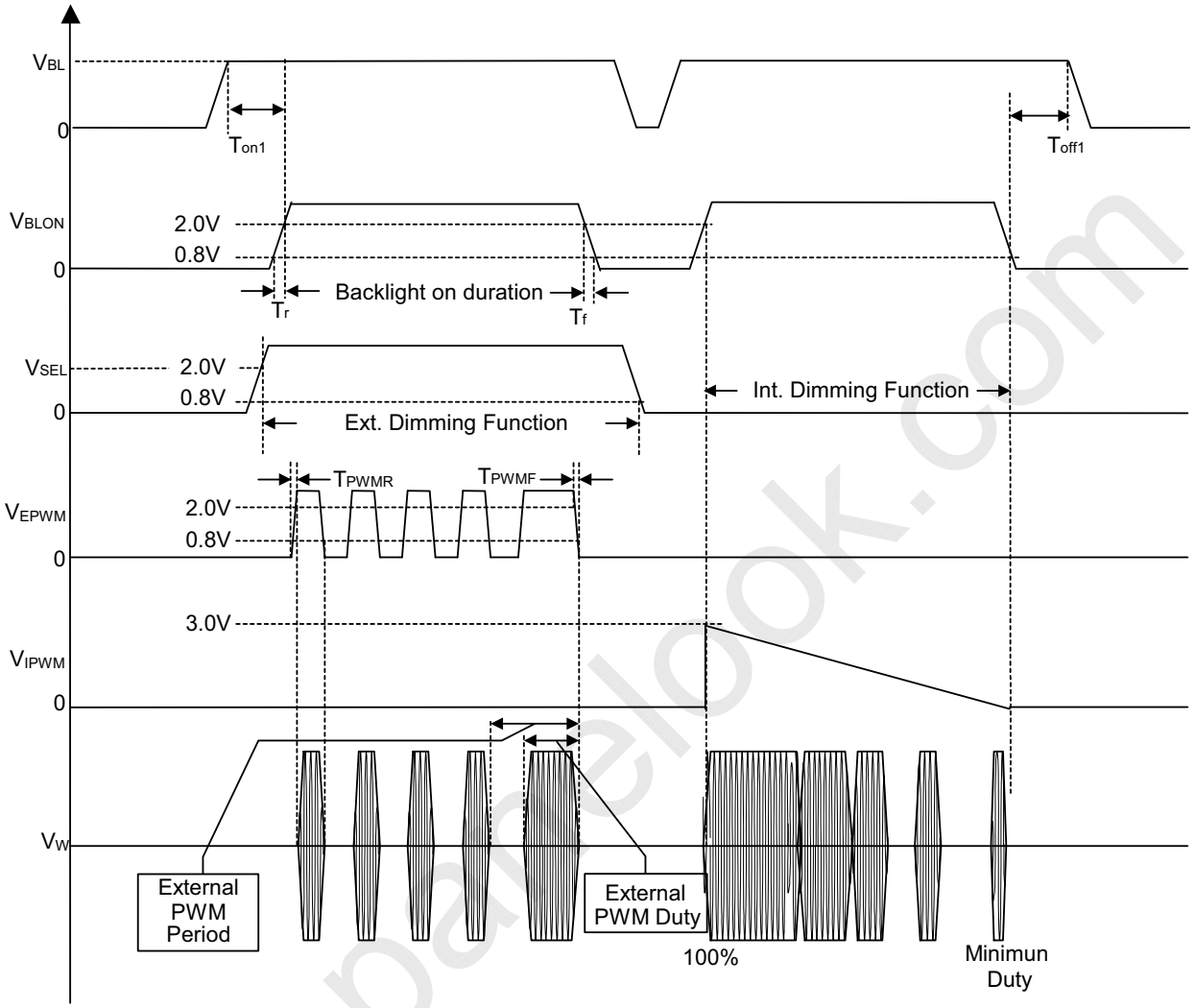
4.2.3 INVERTER INTERTFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal/External PWM Select Voltage	HI	V_{SEL}	—	2.0	—-	5.0	V	
	LO		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	V_{SEL} = L	—	—	3.0	V	maximum duty ratio
	MIN			—	0	—	V	minimum duty ratio
External PWM Control Voltage	HI	V_{EPWM}	V_{SEL} = H	2.0	—	5.0	V	duty on
	LO			0	—	0.8	V	duty off
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		T_{PWMR}	—	—	—	50	us	
PWM Signal Falling Time		T_{PWMF}	—	—	—	50	us	
Input impedance		R_{IN}	—	1	—	—	MΩ	
BLON Delay Time		T_{on}	—	1	—	—	ms	
BLON Off Time		T_{off}	—	1	—	—	ms	

Note (1) The SEL signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM selection (SEL) during backlight turn on period.

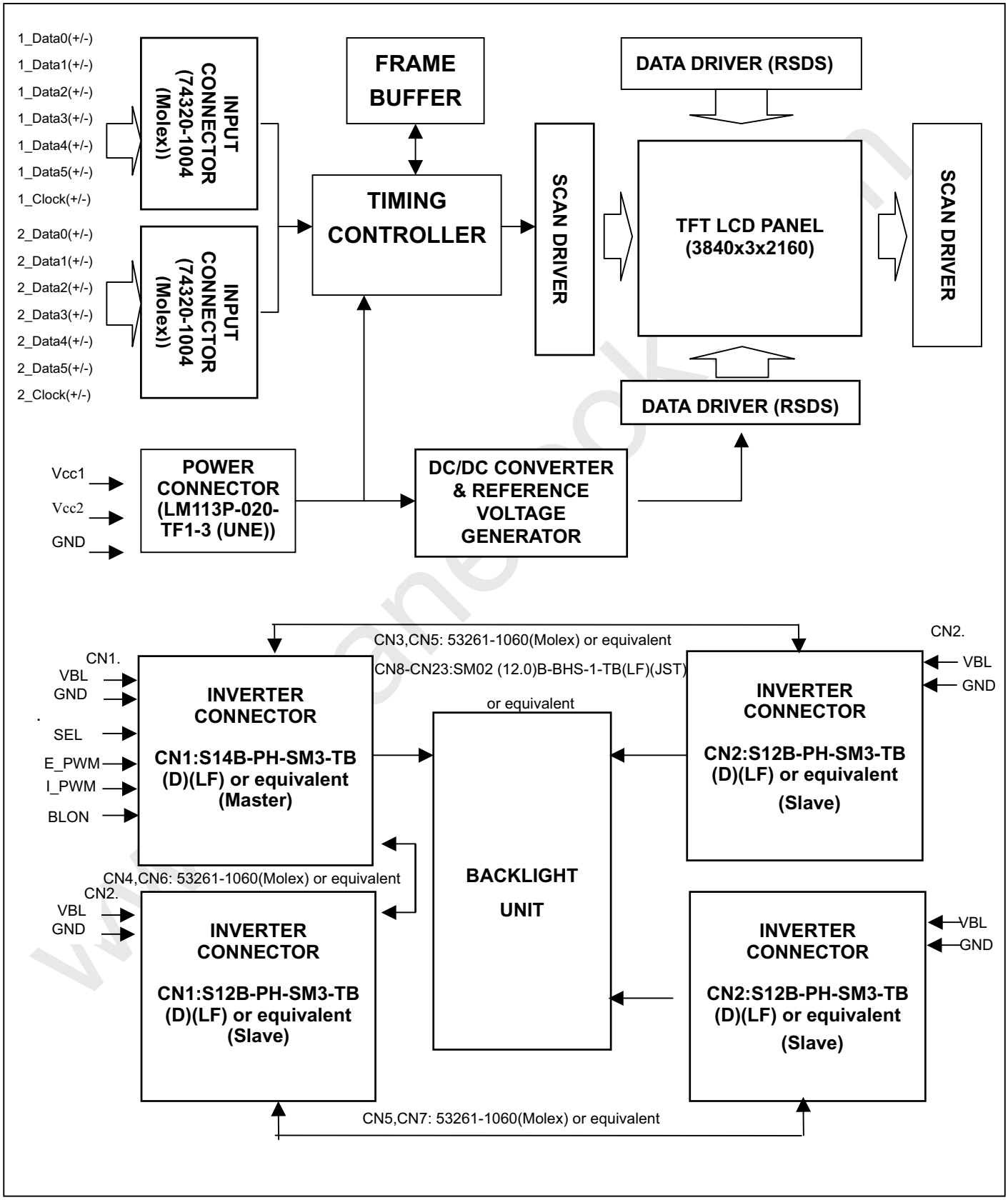
Note (2) The power sequence and control signal timing are shown in the following figure.

Note (3) The power sequence and control signal timing must follow the figure below. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.



5. BLOCK DIAGRAM

5.1 TFT LCD MODULE



6. LCD INPUT TERMINAL PIN ASSIGNMENT

6.1 TFT LCD MODULE DVI input

CN6, CN7 Connector Pin Assignment

Pin	Signal Assignment	Pin	Signal Assignment	Pin	Signal Assignment
1	T.M.D.S Data2-	9	T.M.D.S Data1-	17	T.M.D.S Data0-
2	T.M.D.S Data2+	10	T.M.D.S Data1+	18	T.M.D.S Data0+
3	T.M.D.S Data2/4 shield	11	T.M.D.S Data1/3 shield	19	T.M.D.S Data0/5 shield
4	T.M.D.S Data4-	12	T.M.D.S Data3-	20	T.M.D.S Data5-
5	T.M.D.S Data4+	13	T.M.D.S Data3+	21	T.M.D.S Data5+
6	DDC Clock	14	+5V Power	22	T.M.D.S Clock shield
7	DDC Data	15	Ground(for +5V)	23	T.M.D.S Clock+
8	No Connect	16	Hot Plug Detect	24	T.M.D.S Clock-

Note: CN6, CN7 Connector part no.: 74320-1004 (Molex) or equivalent.

6.2 TFT LCD MODULE Power input

CN9 Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	VIN	+18.0V power supply	(1)
2	VIN	+18.0V power supply	
3	VIN	+18.0V power supply	
4	V5VC	+5.0V power supply	
5	V5VC	+5.0V power supply	
6	V5VC	+5.0V power supply	
7	V5VC	+5.0V power supply	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	GND	Ground	
12	GND	Ground	
13	GND	Ground	
14	GND	Ground	
15	NC	Not connection	
16	NC	Not connection	
17	NC	Not connection	
18	NC	Not connection	
19	NC	Not connection	
20	NC	Not connection	

Note: (1) CN9 Connector part no.: LM113P-020-TF1-3,UNE(高麟蘇州) or equivalent.

(2) CN10 approve for CMO

6.3 BACKLIGHT UNIT

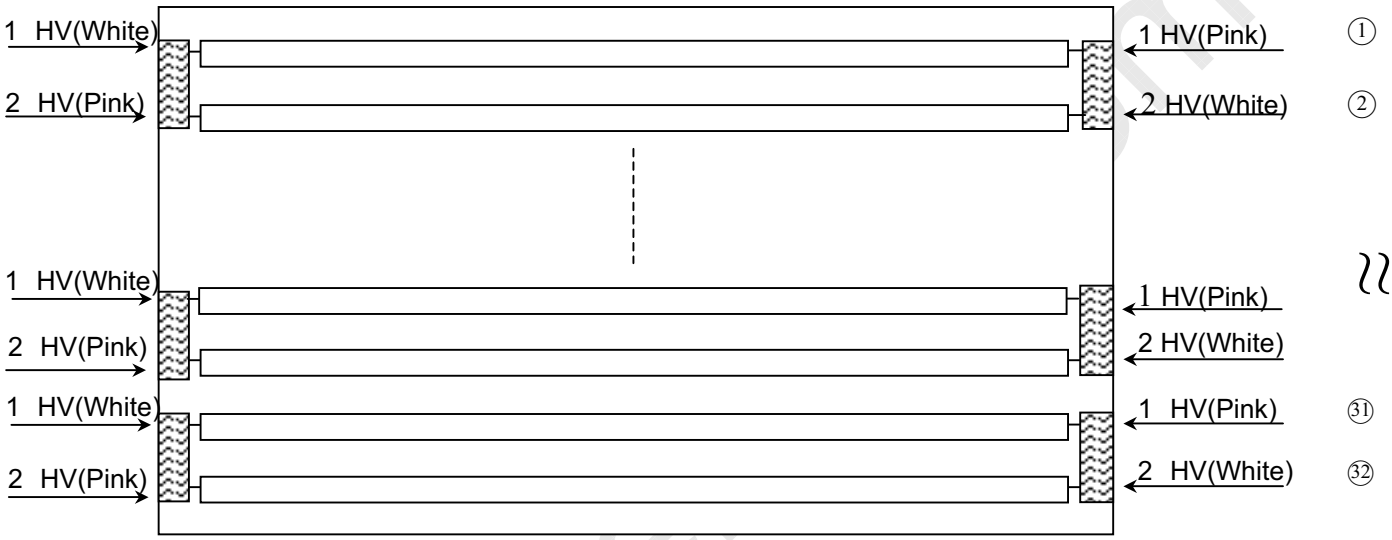
The pin configuration for the housing and the leader wire is shown in the table below.

CN8-CN23: BHR-04VS-1 (JST).

Pin	Name	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-04VS-1, manufactured by JST.

The mating header on inverter part number is SM02(12.0)B-BHS-1-TB(LF).



6.4 INVERTER UNIT

CN1(Master, Header): S14B-PH-SM3-TB(D)(LF)(JST) or equivalent

Pin No.	Symbol	Description
1	VBL	+24V_{DC} power input
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	SEL	Internal/external PWM selection High : external dimming Low : internal dimming
12	E_PWM	External PWM control signal E_PWM should be connected to ground when internal PWM was selected (SEL = Low).
13	I_PWM	Internal PWM Control Signal I_PWM should be connected to ground when external PWM was selected (SEL = High).
14	BLON	Backlight on/off control

CN2(Slave, Header): S12B-PH-SM3-TB(D)(LF)(JST) or equivalent

Pin No.	Symbol	Description
1	VBL	+24V_{DC} power input
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	NC	NC

CN8-CN15(Master, Header), CN16-CN23(Slave, Header): SM02(12.0)B-BHS-1-TB(LF)(JST) or equivalent

Pin No.	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

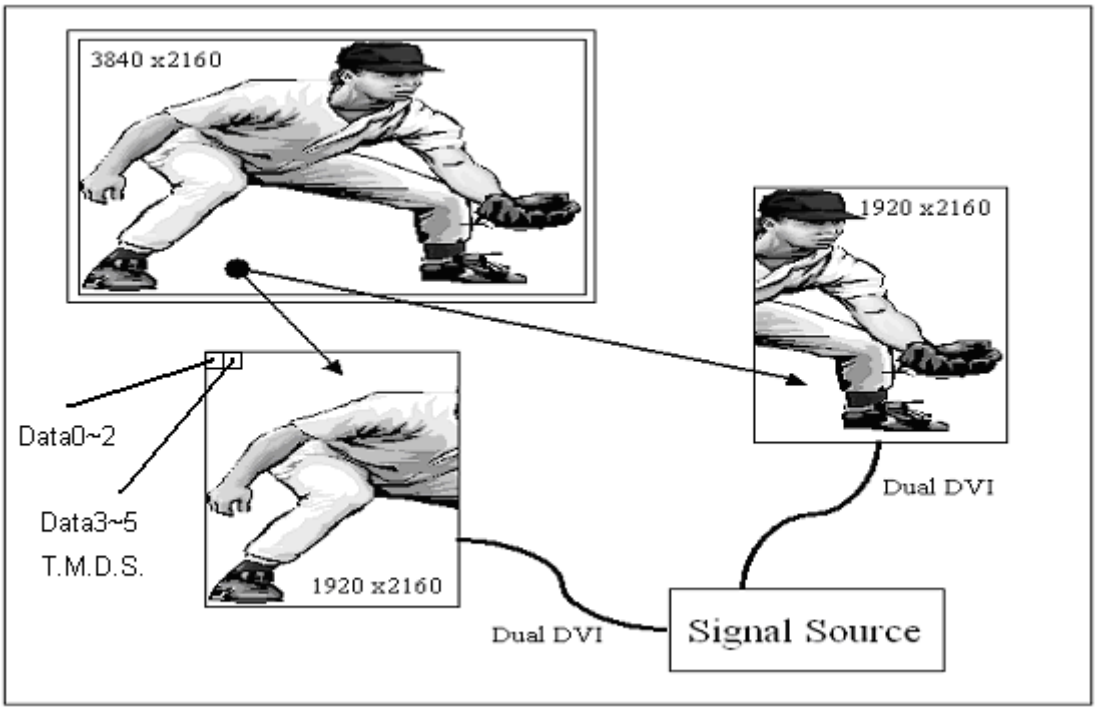
CN3-CN4(Master, Header),CN5-CN7(Slaver, Header): 53261-1060(Molex) or equivalent

Pin No.	Symbol	Description
1	Control Signal	Board to Board
2		Board to Board
3		Board to Board
4		Board to Board
5		Board to Board
6		Board to Board
7		Board to Board
8		Board to Board
9		Board to Board
10		Board to Board

Note (1) Floating of any control signal is not allowed.

6.5 BLOCK DIAGRAM OF INTERFACE

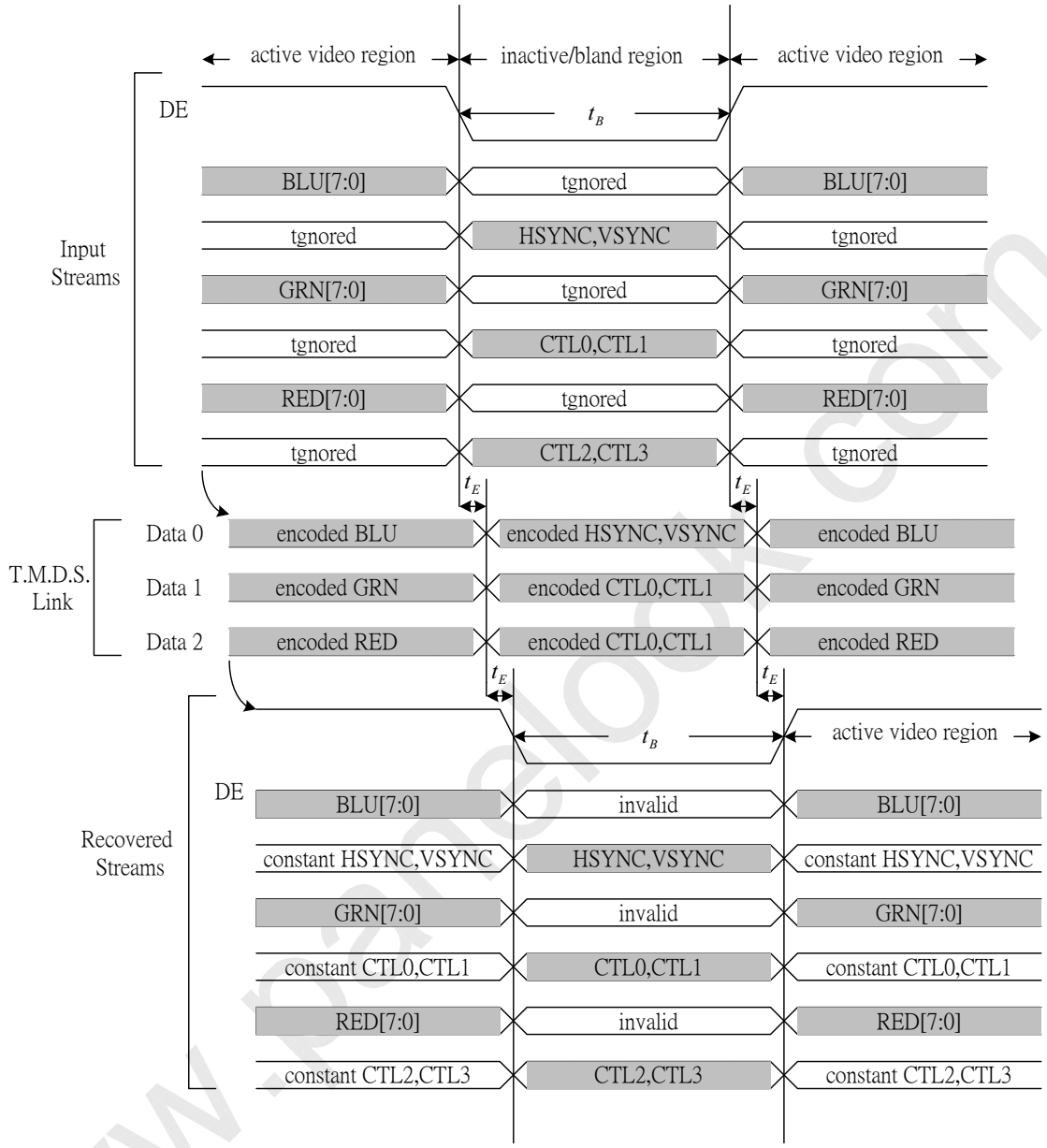
The video picture (3840x2160) should be to divide to two parts : the left side(1920x2160) and the right side(1920x2160). Each pattern should be send through the dual-DVI interface and the protocol specified in the DVI interface specification of DDWG.



6.6 DVI INTERFACE

Signal Name	Signal Description
T.M.D.S. Signals	
T.M.D.S. Clock + & -	T.M.D.S. clock differential pair.
T.M.D.S. Clock Shield	Shield for T.M.D.S. clock differential pair.
T.M.D.S. Data0 + & -	T.M.D.S. link #0 channel #0 differential pair.
T.M.D.S. Data0/5 Shield	Shared shield for T.M.D.S. link #0 channel #0 and link #1 channel #2.
T.M.D.S. Data1 + & -	T.M.D.S. link #0 channel #1 differential pair.
T.M.D.S. Data2/4 Shield	Shared shield for T.M.D.S. link #0 channel #2 and link #1 channel #1.
T.M.D.S. Data2 + & -	T.M.D.S. link #0 channel #2 differential pair.
T.M.D.S. Data1/3 Shield	Shared shield for T.M.D.S. link #0 channel #1 and link #1 channel #0.
T.M.D.S. Data3 + & -	T.M.D.S. link #1 channel #0 differential pair.
T.M.D.S. Data4 + & -	T.M.D.S. link #1 channel #1 differential pair.
T.M.D.S. Data5 + & -	T.M.D.S. link #1 channel #2 differential pair.
Control Signals	
Hot Plug Detect(HPD)	Signal is driven by monitor to enable the system to identify the presence of a monitor.
DDC Data	The data line for the DDC interface.
DDC Clock	The clock line for the DDC interface
+5V Power	+5 volt signal provided by the system to enable the monitor to provide EDID data when the monitor circuitry is not powered.
Ground (for +5V)	Ground reference for +5 volt power pin. Used as return by Hsync and Vsync Signals.
Analog Signals	
Analog Red	Analog Red signal.
Analog Green	Analog Green signal.
Analog Blue	Analog Blue signal.
Analog Horizontal Sync	Horizontal synchronization signal for the analog interface.
Analog Vertical Sync	Vertical synchronization signal for the analog interface.
Analog Ground	Common ground for analog signals. Used as a return for analog red, green and blue signals only.

6.7 DVI INTERFACE LINK TIMMING



Symbol	Description	Value	Unit
t_B	Minimum duration blanking period required to ensure character boundary recovery at the receiver. Blanking periods of this duration must occur at least once every 50mS (20Hz).	128	T_{pixel}
t_E	Maximum encoding/serializer pipeline delay.	64	T_{pixel}
t_R	Maximum recovery/de-serizlizer pipeline delay. Recovery timing includes inter-channel skew, and is measured from the earliest DE transition among the data channels.	64	T_{pixel}

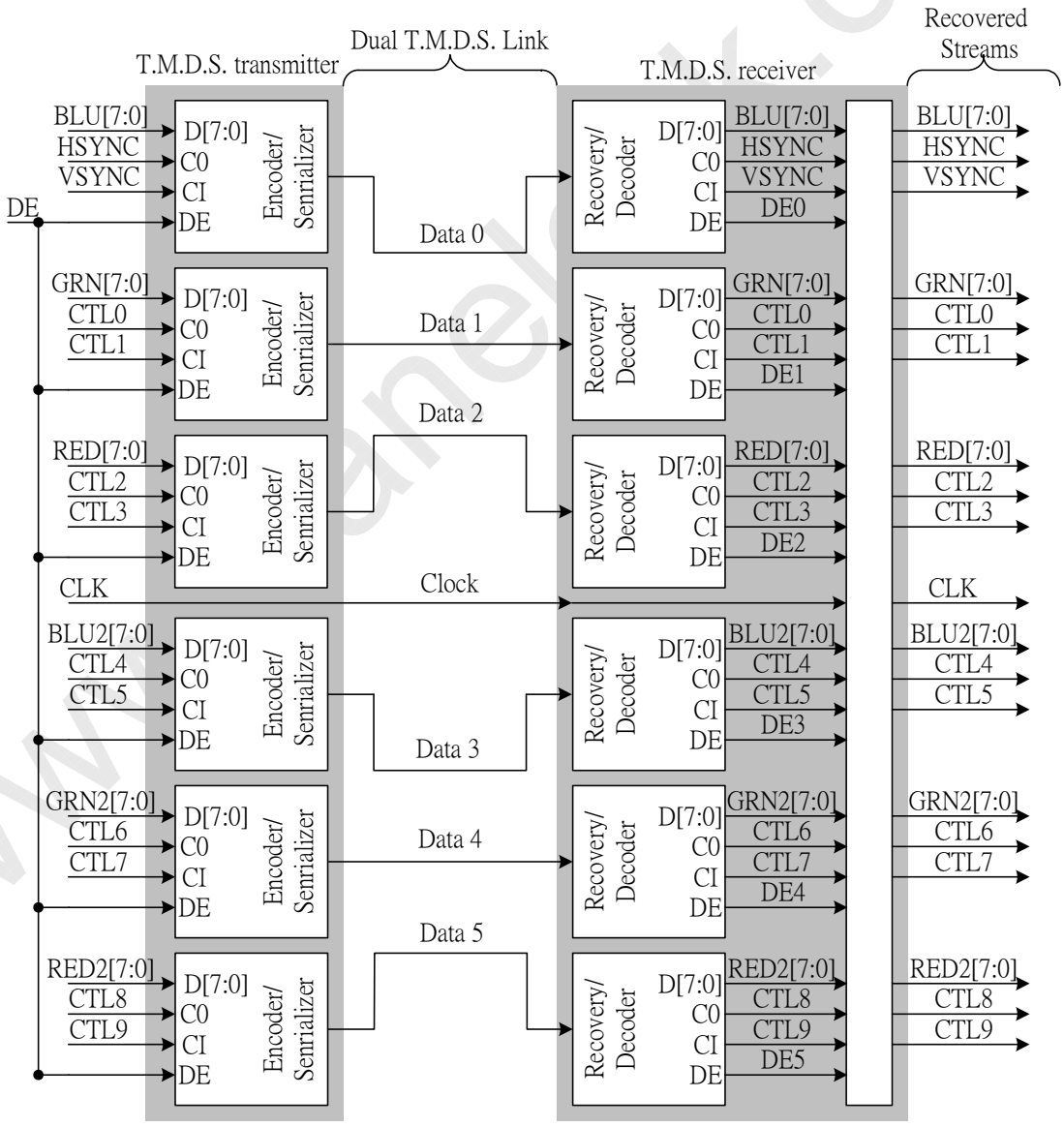
7. INTERFACE TIMING

7.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DVI Receiver Clock	Frequency	1/Tc	(130)	152	(156)	MHz	
Vertical Active Display Term	Frame Rate	Fr6	47	50	53	Hz	
	Total	Tv	(2164)	2168	(2320)	Th	Tv=Tvd+Tvb
	Display	Tvd	-	2160	-	Th	
	Blank	Tvb	(4)	8	(160)	Th	
Horizontal Active Display Term	Total	Th	(4696)	4700	(4900)	Tc	Th=Thd+Thb
	Display	Thd	-	3840	-	Tc	
	Blank	Thb	(856)	860	(1060)	Tc	

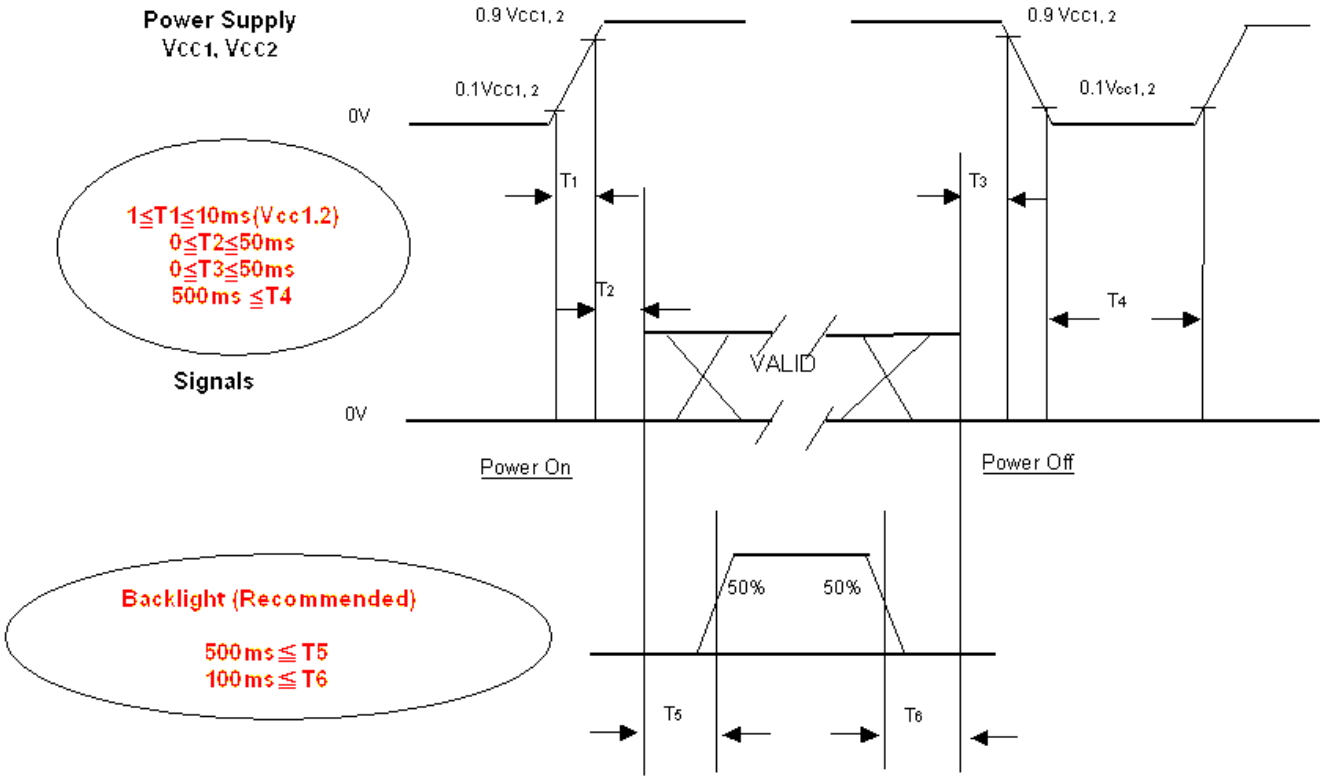
Note: (1) Since this module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.



Notes: The TMDS protocol of DVI interface are specified in the DVI interface specification of DDWG

7.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



Power ON/OFF Sequence

Note : (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

(2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

8. OPTICAL CHARACTERISTICS

8.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	6.5±0.5	mA
Oscillating Frequency (Inverter)	F_L	50±3	KHz
Frame Rate	F_r	60	Hz

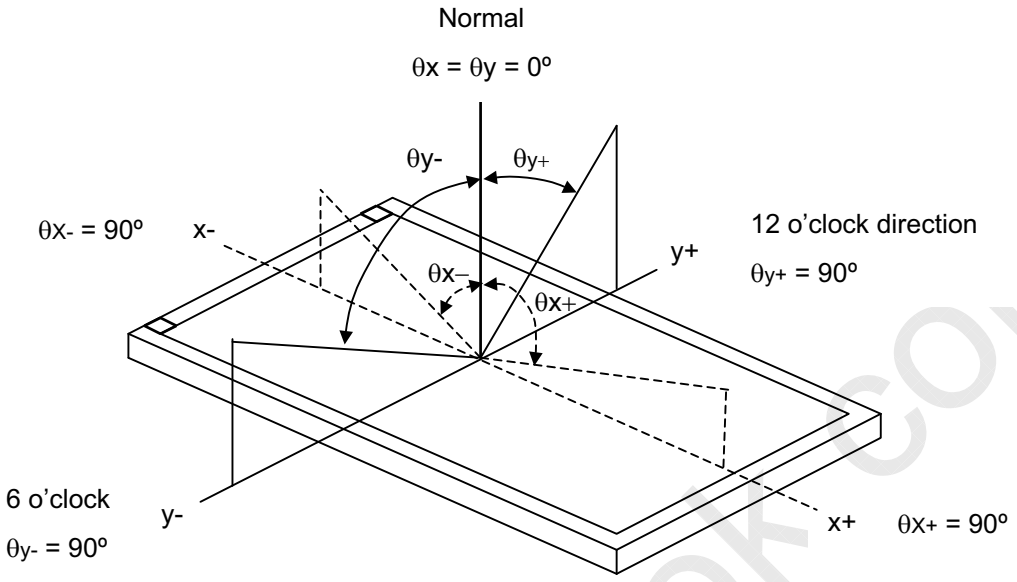
8.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle		(1200)		-	Note (2)
Response Time		Gray to gray			(6.5)		ms	Note (3)
Center Luminance of White		L_C			(500)		cd/m^2	Note (4)
Average Luminance of White		L_{AVE}			(450)	-	cd/m^2	Note (4)
White Variation		δW				(1.6)	-	Note (7)
Cross Talk		CT				(4)	%	Note (5)
Color Chromaticity	Red	Rx		Typ. -0.03	(0.652)	Typ. +0.03	-	Note (6)
		Ry			(0.332)		-	
	Green	Gx			(0.275)		-	
		Gy			(0.601)		-	
	Blue	Bx			(0.142)		-	
		By			(0.065)		-	
	White	Wx			0.285		-	
		Wy			0.293		-	
	Color Gamut	C.G		(72)	75		%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥30	(80)	(88)		Deg.	Note (1)
		θ_x-		(80)	(88)			
	Vertical	θ_Y+		(80)	(88)			
		θ_Y-		(80)	(88)			

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

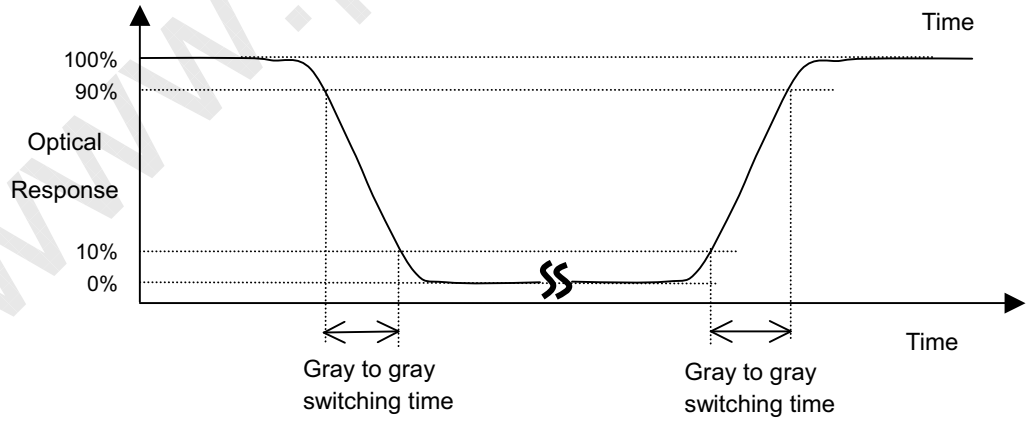
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time:



The driving signal means the signal of gray level 0, 63, 127, 191, 255.

Gray to gray average time means the average switching time of gray level 0 ,63,127,191,255 to each other.

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$

$L_{AVE} = [L(1)+ L(2)+ L(3)+ L(4)+ L(5)] / 5$

Where L (x) is corresponding to the luminance of the point X at the figure in Note (7).

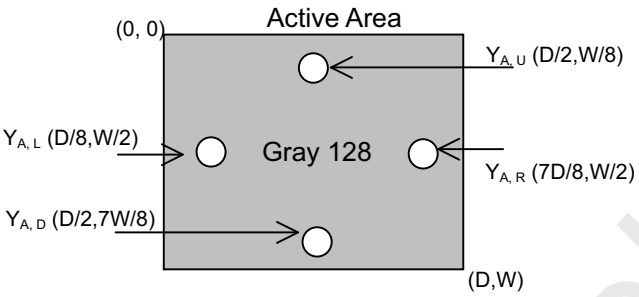
Note (5) Definition of Cross Talk (CT):

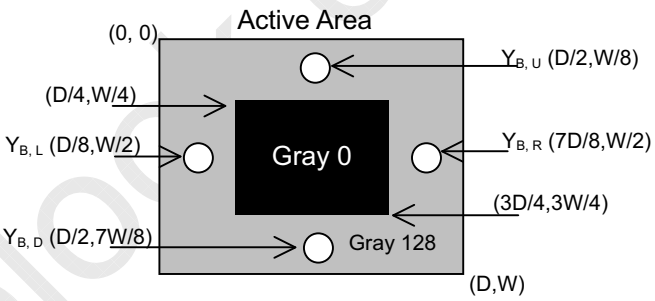
$CT = | Y_B – Y_A | / Y_A \times 100\ (\%)$

Where:

Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

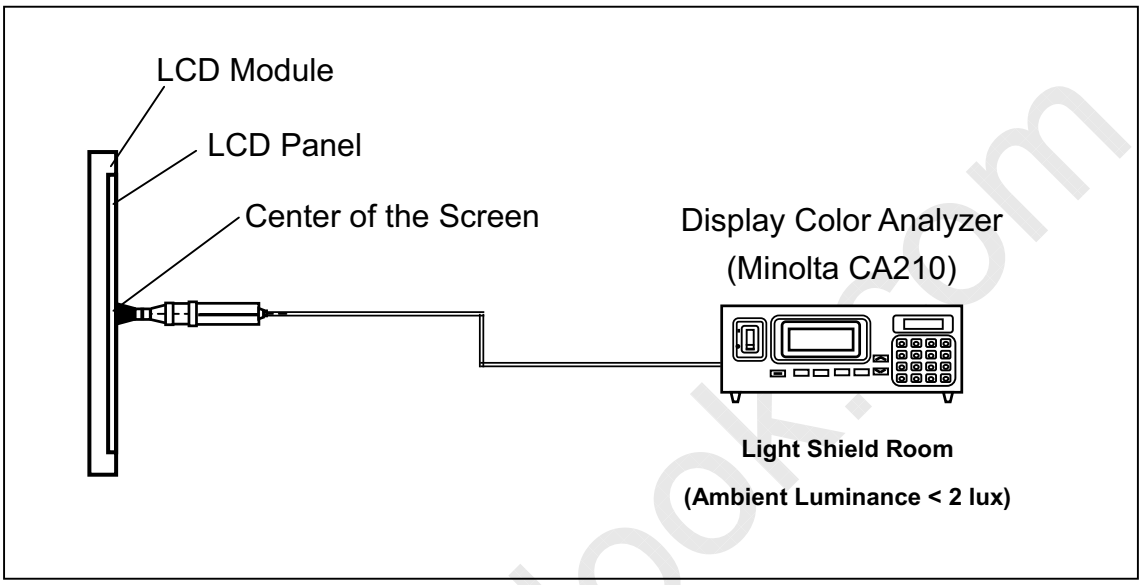
Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)





Note (6) Measurement Setup:

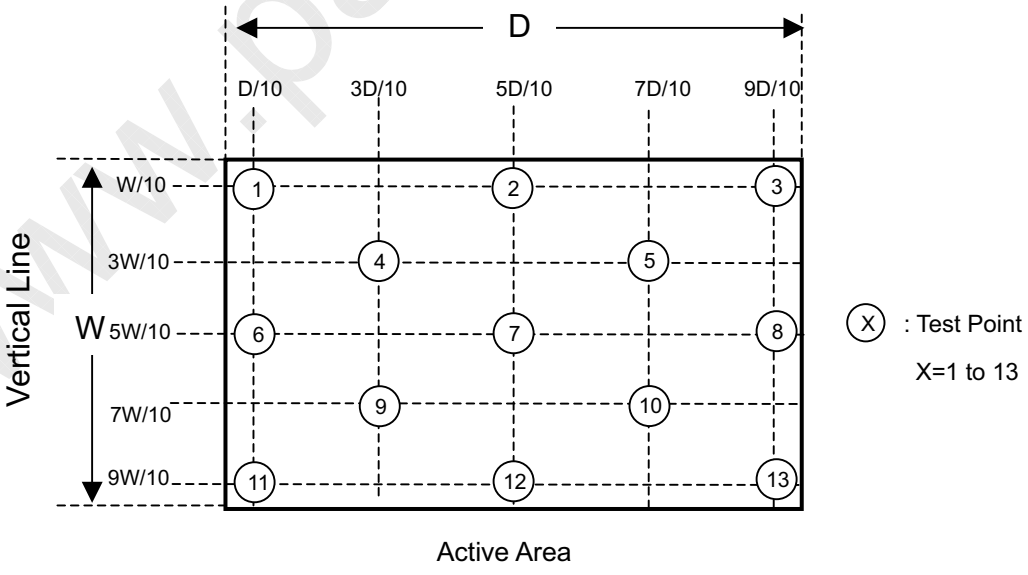
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), 、、、, L (13)] / Minimum [L (1), L (2), L (3), L (4), 、、、, L (13)]



9. PRECAUTIONS

9.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) When storing modules as spares for a long time, the following precaution is necessary.

a. Do not leave the module in high temperature, and high humidity for a long time.It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

b. The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

9.2 SAFETY PRECAUTIONS

(1) The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

9.3 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

(1) UL60950-1 or updated standard.

(2) IEC60950-1 or updated standard.

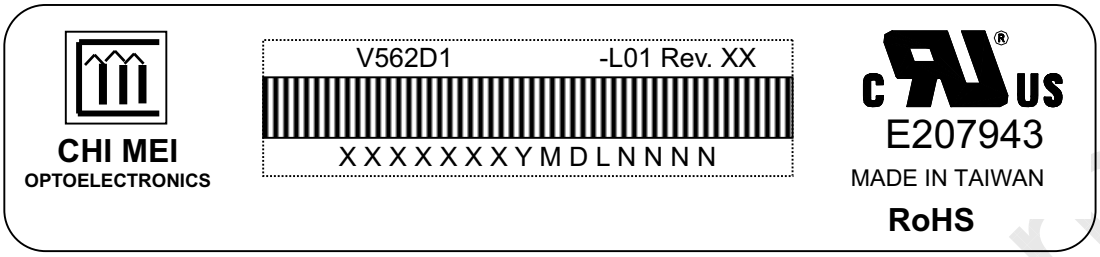
(3) UL60065 or updated standard.

(4) IEC60065 or updated standard.

10. DEFINITION OF LABELS

10.1 CMO MODULE LABEL

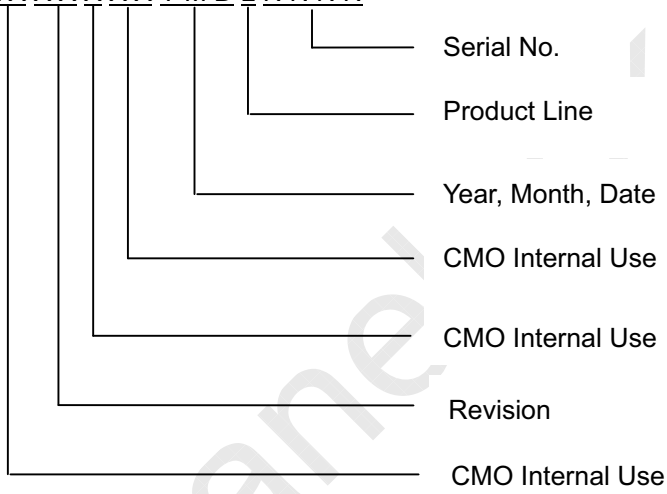
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V562D1-L01

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2000~2009
Month: 1~9, A~C, for Jan. ~ Dec.
Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

11. PACKAGE

11.1 PACKING SPECIFICATIONS

(1) 2 LCD TV modules / 1 Box

(2) Box dimensions : 1448(L) X 372 (W) X 901 (H)

(3) Weight : approximately 56Kg (2 modules per box)

11.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

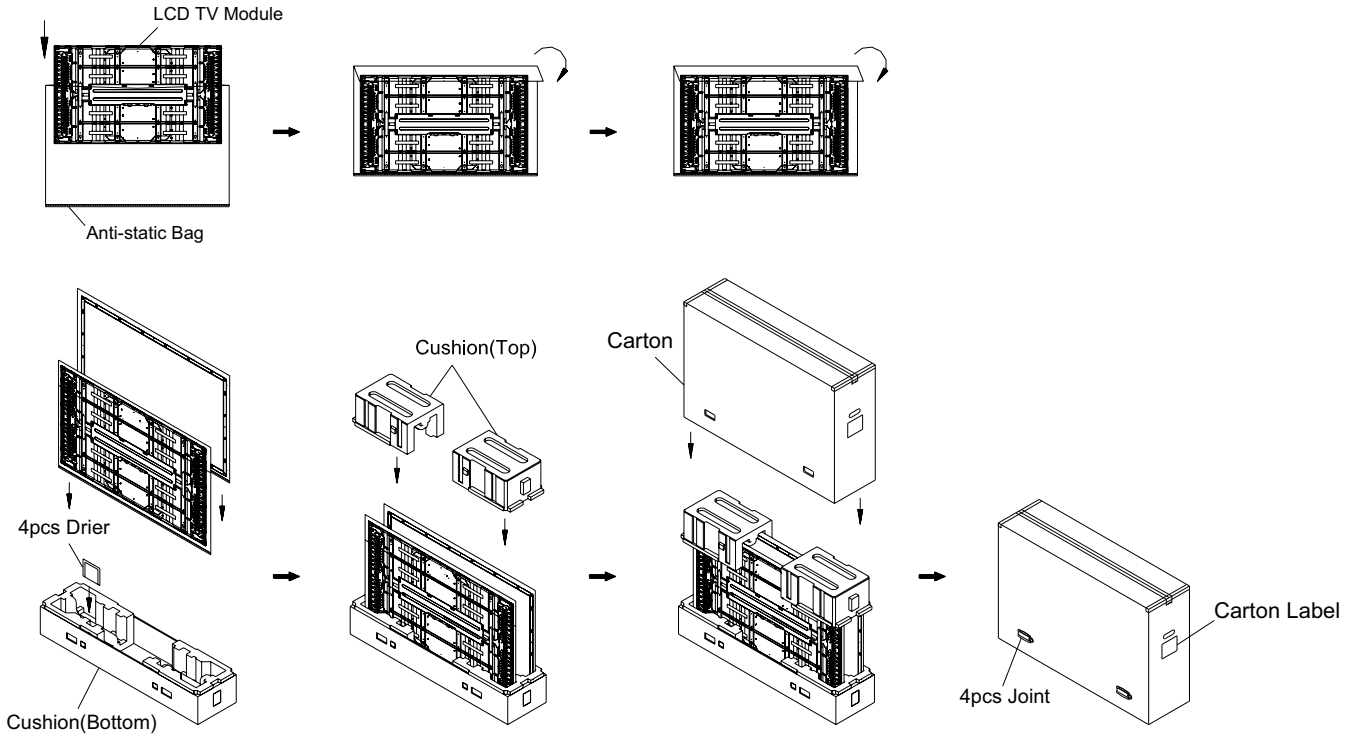
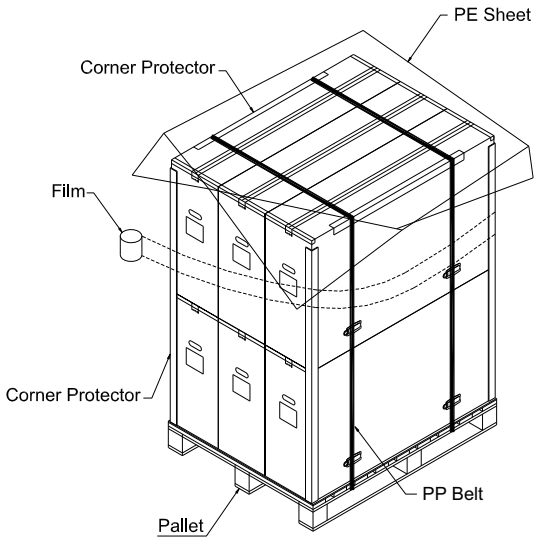


Figure.9-1 packing method

Sea Transportation

Corner Protector:L1780*50mm*50mm
Corner Protector:L1130*50mm*50mm
Pallet:L1150*W1460*H140mm
Pallet Stack:L1150*W1460*H1942mm
Gross:353kg



Air Transportation

Corner Protector:L800*50mm*50mm
Corner Protector:L1130*50mm*50mm
Pallet:L1150*W1460*H140mm
Pallet Stack:L1150*W1460*H1041mm
Gross:185kg

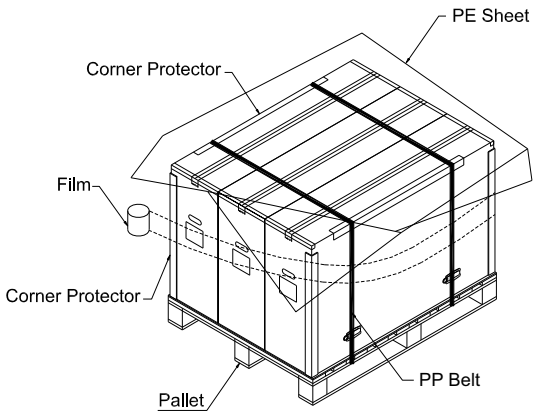


Figure. 9-2 Packing method

12. MECHANICAL CHARACTERISTIC